F-15(1D-45)

PDP 1

SUPPLEMENT

(PDP-1D-45)

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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FOREWORD

This supplement describes special instructions added to PDP-1D-45 at Bolt Beranek and Newman. They are grouped as follows:

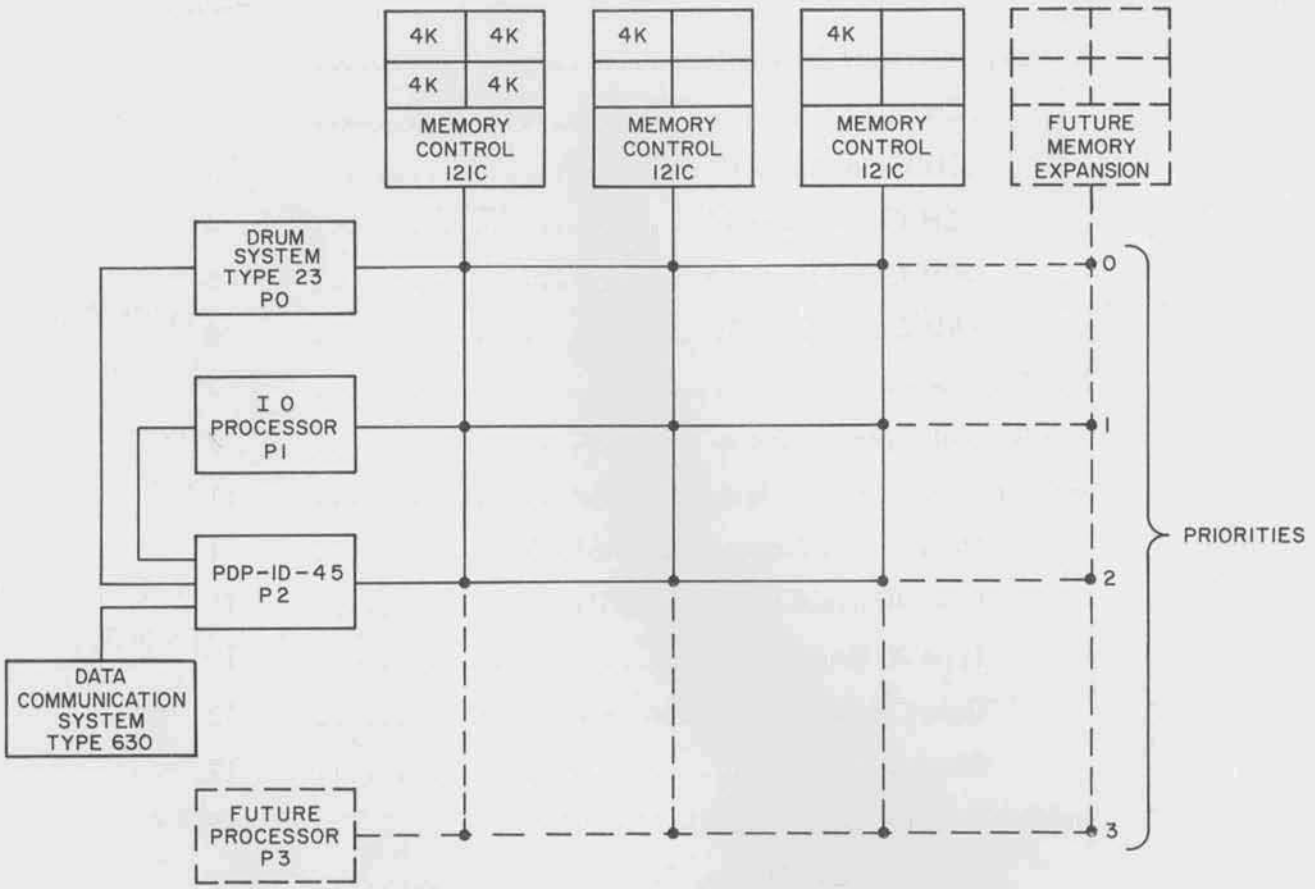
Memory Reference Instructions
- Load Character (LCH)
- Deposit Character (DCH)
- Twos Complement Add (TAD)

The Skip Group

The Special Operate Group

The Input-Output Transfer Group

CONTENTS



PDP-ID-45 SYSTEM

MEMORY REFERENCE INSTRUCTIONS

LCH - Octal Code 12 - Load accumulator with a character from memory.

DCH - Octal Code 14 - Deposit a character from accumulator in memory.

Each of these instructions is interpreted as being deferred, hence requiring three memory cycles for execution. The MB and AC are divided into three sections of six bits each. Bits 0-5 = character one (1), bits 6-11 = character two (2), and bits 12-17 = character three (3).

The instructions are sub-decoded from MB bits 0 and 1 during the defer cycle. MB bits 0 and 1 are placed in the load-deposit register (LD) and decoded:

Octal Code 12 and LD - 01 = LC1 - Load character one loads accumulator from memory bits 0-5 and places in accumulator bits 0-5. (AC_{0-5})

Octal Code 12 and LD - 10 = LC2 - Load character two loads accumulator from memory bits 6-11, and shifts into AC bits 0-5.

Octal Code 12 and LD - 11 = LC3 - Load character three loads accumulator from memory bits 12-17, and shifts into AC bits 0-5.

Octal Code 14 and LD - 01 = DC1 - Deposit character one deposits accumulator bits 0-5 in memory bits 0-5.

Octal Code 14 and LD - 10 = DC2 - Deposit character two deposits accumulator bits 0-5 in memory bits 6-11.

Octal Code 14 and LD - 11 = DC3 - Deposit character three deposits accumulator bits 0-5 in memory bits 12-17.

LCH

The registers below show a single step sequence through the LCH instruction if 100_8 is the starting location, and it contains a 12_8 to address 1000_8. The LCH instruction automatically forces a defer cycle. During the defer cycle, the memory address (MA) contains 1000_8, and the contents of the MB contain a 01 in the XX position and 2000_8 in the address portion of the

MB. During cycle one, 2000_8 would be the address. If the MB at this time is assumed to contain A, B, and C, the character A is transferred into the accumulator and the remaining 12 bits are cleared as shown in Figure a. During the defer cycle, if the XX portion of the MB contains 10, the character is transferred into the accumulator and the last 12 bits are cleared as shown in Figure b. If the XX portion of the MB contains 11 during the defer cycle, the results would appear as shown in Figure c.

CYCLE ZERO

MA

000	001	000	000

MB

001	010	001	000	000	000

DEFER CYCLE

001	000	000	000

XX0	000	010	000	000	000

CYCLE ONE

010	000	000	000

A		B		C	
110	001	110	010	110	011

ACCUMULATOR

Figure a

A					
110	001	000	000	000	000

Figure b

B					
110	010	000	000	000	000

Figure c

C					
110	011	000	000	000	000

The LCH instruction clears AC bits 6-17 and leaves the single character in AC bits 0-5.

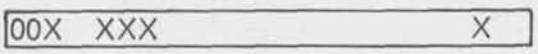
XXX	XXX	000	000	000	000

LCH Octal Code 13

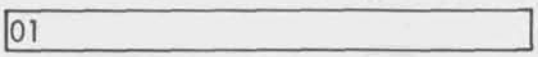
001	01	1	

When the defer bit is a 1 during cycle zero, it sets a one to the increment flip-flop (INC) placing the instruction in the automatic increment mode. In the defer cycle, this takes the first two bits of the MB and effectively adds one (+1) to them. The first time this is used or to enter the automatic mode, the first two bits of the MB should be zeros as the incrementing takes place before the character handling cycle (cycle one).

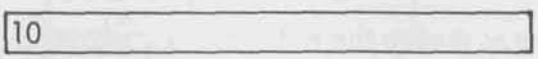
When entering the defer cycle if the address contains a:



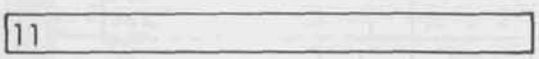
It is incremented to contain:



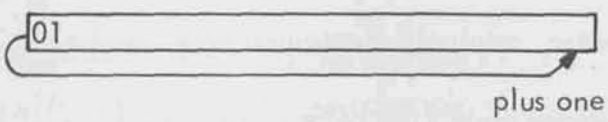
If entered with a 01, it is incremented to:



A 10 is incremented to a:



In the last situation, an 11 causes the character bits to be forced to a 01 and the address portion of the MB to be incremented by one.



Summary: In the automatic mode a sequence performs as follows:

00 - Loads character one
01 - Loads character two
10 - Loads character three
11 - Increments the address (+1) and loads character one in the new address
01 - Character two
10 - Character three
11 - Plus one to address and loads character one in new address
01 - Character two
10 - Character three
11 - Plus one to address and loads character one in new address

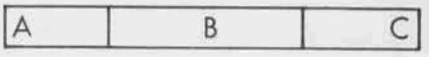
NOTE: If the automatic mode is entered with a 01 in the first two bits of the memory location brought out during the defer cycle, the first character is skipped.

If a 00 is used in the non-automatic instruction, it is interpreted as a LC1 (01) and loads the accumulator from memory bits 0-5.

In the automatic mode a mid-instruction break is not allowed between the defer cycle and cycle one. (No sequence breaks can occur between the defer cycle and cycle one).

DCH Octal Code 14

Assuming a sequence of cycles as used in the LCH instruction, if the accumulator contains a series of characters thus:

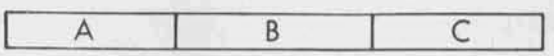


and the memory location addressed during the defer cycle contains a DC1 (01) in the first two bits, at the end of cycle one the AC would contain:

The MB:

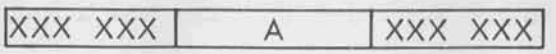
The X's indicate the information originally contained here remains unchanged.

If the memory location addressed during the defer cycle contains a DC2 (10), and the AC initially contains

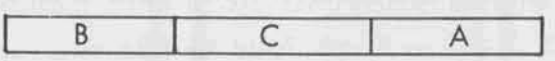


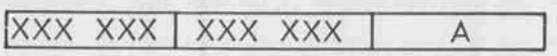
The result in the AC would be

In the MB



A DC3 (11) provides the following results in the AC and MB if the AC initially contains the ABC.

AC 

MB 

The following is the result left in the AC and MB if a sequence of DCH instructions is used (non-automatic) and the AC initially contains an ABC in that order:

DC1

AC	B	C	A
MB	A	X	X

DC2

AC	C	A	B
MB	A	B	X

DC3

AC	A	B	C
MB	A	B	C

Summary: The DCH instruction always takes the character that is in the first six bits of the AC and places it in the character position designated by the first two bits decoded in the defer cycle: first character to first position, first character to second position, or first character to third position.

DCH Octal Code 15

The DCH instruction, using the indirect address bit (bit 5) of the word as a 1, sets the INC flip-flop and during the defer cycle increments the sub-instruction through the same sequence as shown for LCH. The automatic mode should be entered with a 00 in the location addressed in the defer cycle. (Reference from AC to MB)

DCH 00 - Deposits first character in first position.
DCH 01 - Deposits first character in second position.
DCH 10 - Deposits first character in third position.
DCH 11 - Increments the address and deposits the first character in the first position of the new address.

If the alphabet were typed in by a program sequence it might resemble this:

```
Start    cla V clf        /clear accumulator and flag 1
         szf i (1)        /listen loop
         jmp.-1
         tyi              /bring in typed character
         rcr (6)          /move from I/O to AC
         sad (77)         /compare for end character (77)
         hlt
         dch i store
         jmp start
```

The MB storage locations would be packed thus:

1	A	B	C
2	D	E	F
3	G	H	I
4	J	K	L
5	M	N	O
6	P	Q	R
7	S	T	U
10	V	W	X
11	Y	Z	

Summary: The DCH instruction deposits the accumulator bits 0-5 into the character location of the memory buffer specified by the bits 0, 1 of the location addressed in the defer cycle, and rotates the next character or that character contained in accumulator bits 6-11 into accumulator bits 0-5 so that it might be deposited in memory on the next use of this same DCH instruction.

If the automatic mode is entered with other than a 00, a character is skipped. A 00 used in the non-automatic mode is interpreted as a 01.

TAD Octal Code 36

TAD - 2's complement add

The state of the link is sensed, and if a ONE, one is added to the AC (+1 to AC). The C(Y) are then added to the C(AC). The result is left in the AC and the original C(AC) are lost. The C(Y) are unchanged. A carry out of bit 0 is retained in the link flip-flop.